Claim 30 recites the feature of a controller that renews recording results of a determination of completion of each stage of rewriting processing or results of a determination of whether each stage is good or bad into flag areas a step at a time. Applicant submits that the cited prior art fails to teach or suggest at least this feature of claim 30.

For example, to the extent that the Examiner applies Watanabe et al. (US 5,590,306) to newly submitted claims 30-39, Applicant submits the following. Watanabe discloses data packets having a read protect bit which is able to hold values of either " 0" or "1" (see column 11, lines 51-54). In Watanabe, when a writing process begins, a read protect bit is set to "1" (see column 16, lines 24-29). If the writing process is successful, the read protect bit is changed from "1" to "0" (see column 16, lines 29-32). However, if an error occurs during writing (e.g., the memory card is ejected during the writing operation), the read protect bit retains a value of "1" because the writing process never completed (see column 16, lines 32-36). Thus, the system is able to determine which packets did not undergo a successful writing operation by monitoring which data packets have a read protect bit value of "1" (see column 16, lines 36-38).

Based on the foregoing, Applicant submits that Watanabe merely discloses a system that is able to determine if a rewriting process was performed without interruption by comparing a bit value of a data packet to an expected bit value. Watanabe, however, does not disclose or suggest a controller that renews recording results of a determination of completion of each stage of rewriting processing or results of a determination of whether each stage is good or bad into flag areas a step at a time, as set forth in claim 30.

Accordingly, as Watanabe fails to disclose or suggest all of the features of claim 30, Applicant respectfully requests that the rejection be reconsidered and withdrawn. Claim 31 depends from claim 30 and therefore incorporates all of the features thereof. Accordingly, Applicant submits that claim 31 is patentable at least by virtue of its dependency.

Independent claim 32 recites the feature of a controller that determines completion of a plurality of stages of rewriting processing or determination of whether the plurality of stages are good or bad and records results of the determination into flag areas and a controller that writes an expected value when rewriting is completed regularly in a flag area at the last stage of rewriting processing and changes the expected value at the first stage of rewriting processing. For at least the same reasons as discussed above with respect to claim 30, Applicant submits that Watanabe fails to disclose or suggest at least this feature of claim 32.

Independent claims 33, 35 and 37-39 recite similar features to those discussed above with respect to claims 30 and 32. Accordingly, Applicant submits that Watanabe also fails to disclose or suggest all of the features of these claims. Claims 34 and 36 depend from claims 33 and 35, respectively. Accordingly, Applicant submits that claims 34 and 35 are patentable at least by virtue of their dependency.

In view of the above, reconsideration and allowance of this application are now believed to be in order, and such actions are hereby solicited. If any points remain in issue which the Examiner feels may be best resolved through a personal or telephone interview, the Examiner is kindly requested to contact the undersigned at the telephone number listed below.

RESPONSE TO COMMUNICATION
U.S. Appln. No. 09/401,293

The USPTO is directed and authorized to charge all required fees, except for the Issue

Fee and the Publication Fee, to Deposit Account No. 19-4880. Please also credit any

overpayments to said Deposit Account.

Respectfully submitted,

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